NAJATH AKRAM, PH.D.

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SUMMARY

An accomplished and driven engineering professional with extensive experience in wireless systems design and project management. Established capabilities in developing wireless communication strategies to enhance product performance and reliability. Effective leader and communicator skilled in delivering scalable solutions that exceed expectations. Leverages excellent technical expertise as well as interpersonal and problem-solving skills to collaborate with team members and achieve operational excellence. Serves as a key contributor to the long-term success of the organization.

EXPERIENCE

JABIL, INC. — Warren, New Jersey

Principal Design Engineer (Wireless Systems) 2023-2024
Lead Design Engineer (Wireless Systems) 2021-2023
Senior FPGA Engineer (Wireless Systems) 2020-2021

- Led cross-functional software and firmware teams in developing wireless communication solutions for LTE and 5G NR O-RAN Remote Radio Units (RRUs), significantly enhancing product performance and reliability.
- Defined 5G NR implementation requirements for projects and guided the digital hardware design team to meet 3GPP specifications with optimized complexity; produced comprehensive architectural and implementation guidance documents.
- Performed filter design, Crest Factor Reduction (CFR) simulation, cancellation pulse generation, and end-to-end system modeling and simulation for uplink, downlink, PRACH Digital Front End (DFE), and LPHY firmware in single, dual, and tri-band LTE / 5G NR (FDD / TDD) radios.
- Generated stimulus test vectors for RTL simulation, integrated Xilinx C-models for hard IPs, and developed executable models for UVM test benches.
- Developed scripts to extract control-plane and user-plane O-RAN data from PCAP files containing Ethernet packets for bit-accurate system modeling.
- Contributed to strategic decision making for massive MIMO implementation on O-RUs and determined O-RAN functional splits to optimize resource allocation and project timelines.
- Conducted in-depth studies on mixed OFDM / OTFS implementations and Passive Intermodulation (PIM) cancellation techniques, leading to improved system efficiency.

FLORIDA INTERNATIONAL UNIVERSITY — Miami, Florida

Graduate Research Assistant 2018-2020

- Developed digital and mixed-domain hardware complexity reduction algorithms for massive MIMO systems, enabling efficient implementations for 5G and emerging 6G networks through innovative resource optimization.
- Implemented digital beamforming array receiver with 800MHz / channel at 28 GHz, reducing ADC consumption by 75% by using an FDM-based approach.
- Proposed a method to reduce ADC requirements by 50% for 2D phased antenna arrays through multidimensional signal processing while maintaining high signal integrity through over-the-air (OTA) testing.
- Conducted research on phased array systems and calibration by using MATLAB and Simulink to implement advanced DSP algorithms on Xilinx RFSoC platforms, including ZCU111, ZCU1275, and ZCU1285 RFSoC evaluation boards.

MATHWORKS — Natick, Massachusetts

Intern 2019

- Won two awards in MathWorks intern hackathon in Fall 2019.
- Enhanced “HDL Verifier” capabilities by optimizing Xilinx Vivado developments.
- Developed and verified Ethernet (PHY interface) IP designs on multiple FPGAs (Artix / Kintex / Virtex).

THE UNIVERSITY OF AKRON — Akron, Ohio
Graduate Research Assistant 2016-2018

- Conducted DARPA and NSF-funded research on digital signal processing systems for multidimensional computational RF systems.
- Implemented Fast Fourier Transform (FFT) and Approximate Discrete Fourier Transform (ADFT) cores for digital beamforming by using approximate DFT methods, significantly decreasing computational complexity while maintaining high beamforming precision.
- Designed multi-dimensional sigma-delta (Σ−Δ) ADC architectures to replace conventional multi-ADC configurations in phased antenna array receivers.

SYNOPSYS, INC. — Colombo, Sri Lanka
Product Verification Intern 2015

- Utilized Spyglass, VHDL, System Verilog, and ASIC Flow with Xilinx FPGA.
- Developed and automated test cases for product verification, using Perl scripts.

EDUCATION

FLORIDA INTERNATIONAL UNIVERSITY, Miami, Florida
Ph.D., Electrical and Computer Engineering, 2020

UNIVERSITY OF RUHUNA, Galle, Sri Lanka
B.S., (Hons.), Electrical and Information Engineering, 2016

NATIONAL INSTITUTE OF BUSINESS MANAGEMENT, Galle, Sri Lanka
A.S., Business Management, 2015

SELECTED PUBLICATIONS

- Digital and Mixed Domain Hardware Reduction Algorithms and Implementations for Massive MIMO, Florida International University, 2021. PhD dissertation.
- Frequency-Multiplexed Array Digitization for MIMO Receivers: 4-Antennas/ADC at 28 GHz on Xilinx ZCU-1285 RF SoC in IEEE Access vol 9, 2021
- Spacetime Frequency-Multiplexed Digital-RF Array Receivers with Reduced ADC Count in IEEE Transactions on Circuits and Systems II: Express Briefs vol 68, 2021.
- Massive-MIMO and Digital Mm-Wave Arrays on RF-SoCs using FDM for M-Fold Increase in Antennas per ADC/DAC in IEEE Space Hardware and Radio Conference (SHaRC), USA, 2021.
- Fast Radix-32 Approximate DFTs for 1024-Beam Digital RF Beamforming in IEEE Access vol 8, 2020.
- A Four-Element Digital Array Receiver at 28 GHz Using a Single Frequency-Multiplexed ADC in IEEE Int. Symp. on Antennas and Propagation and USNC-URSI Radio Science Meeting, USA, 2019.
- A direct-Conversion digital beamforming array receiver with 800 MHz channel bandwidth at 28 GHz using Xilinx RF SoC in IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS), Israel, 2019.
- Sampling H- & V-Polarized Antennas using a Single ADC for Digital Antenna Arrays by Exploiting Multi-Dimensional Signal Processing RF Circuits in IEEE 23rd Int. Conf. on Digital Signal Processing, China, 2018.
- Multiport ADCs for Microwave Focal Plane Array Dish Receivers in IEEE Int. Symp. on Circuits and Systems, Italy, 2018.
- Improving ADC Figure-of-Merit in Wideband Antenna Array Receivers using Multidimensional Space-Time Delta-Sigma Multiport Circuits in IEEE 10th Int. Workshop on Multidimensional (Nd) Systems, Poland, 2017.
- Multi-beam radio frequency (RF) aperture arrays using multiplier less approximate fast Fourier transform (FFT), Univ. of Akron and Federal Univ. of Pernambuco, Brazil, Tech. Rep. AFRL-RY-WP-TR-2017-0144, 2017, sponsored by Air Force Research Laboratory Sensors Directorate, Wright-Patterson Air Force Base, 2017

TECHNICAL SKILLS

MATLAB | Simulink | Xilinx Libraries / FPGA | O-RAN | OFDM | mMIMO | OTFS | Wireless Systems Design | Filter Design
3GPP Standards for RRU | Bit-exact Modeling | Crest-Factor Reduction | Python | VLSI Design | Vivado
VHDL | Verilog | System Verilog | AWR Design Environment

AFFILIATIONS

Tau Beta Pi Engineering Honor Society, 2019-Present
Institute of Electrical and Electronics Engineers (IEEE), Member, 2013-Present